WHAT IS CLAIMED IS:

1. An apparatus comprising:

comparison logic to determine which segment of multiple segments of a block of memory is being addressed by a received index and to generate a physical address of the location in the block of memory for the received index, the comparison logic adapted to compensate for the block of memory having a segment that is non-contiguous with the other segments of the block of memory to logically access the block of memory as a single contiguous block of memory.

2. The apparatus of claim 1, wherein the comparison logic is adapted to compensate for a segment of the block of memory being expandable.

3. The apparatus of claim 1, wherein the apparatus further includes a number of first registers, each first register to contain a value denoting a size of a corresponding segment of the multiple segments of the block of memory.

4. The apparatus of claim 3, wherein the apparatus further includes a number of second registers, each of the second registers to contain a value denoting a starting physical address of an associated segment of the multiple segments of the block of memory.

5. The apparatus of claim 4, wherein the apparatus further includes a comparator responsive to the number of first registers to perform an out of bounds check.

6. The apparatus of claim 5, wherein the comparison logic is adapted to generate the physical address of the location in the block of memory for the received index by using the size of each segment logically preceding the segment determined to be addressed by the received index.

7. The apparatus of claim 5, wherein the comparison logic is adapted to generate the physical address in the block of memory for the received index by adding the received

index to the starting physical address of the segment determined to be addressed by the received index after subtracting the sizes of the segments logically preceding the segment determined to be addressed by the received index.

8. The apparatus of claim 5, wherein the comparison logic further includes an enable register, the enable register containing a bit for each of the multiple segments of the block of memory, each bit denoting whether the associated segment of the multiple segments of the block of memory is enabled, the enable register being software programmable.

9. The apparatus of claim 5, wherein the comparison logic further includes a detector to provide an error signal indicating an attempt to access a segment that is currently not enabled.

10. The apparatus of claim 4, wherein the number of first registers is one first register to contain the value denoting the size of each segment of the multiple segments, the multiple segments having the same size.

11. The apparatus of claim 10, wherein the comparison logic includes a bit shifter responsive to the first register and the received index to select the segment of the block of memory being addressed by the received index.

12. The apparatus of claim 11, wherein the comparison logic further includes a multiplexer responsive to the bit shifter to multiplex the contents from the number of second registers based on select bits from the bit shifter.

13. The apparatus of claim 12, wherein the apparatus further includes:

an enable register, the enable register containing a bit for each of the multiple segments of the block of memory, each bit denoting whether the associated segment of the multiple segments of the block of memory is enabled, the enable register being software programmable; and

a detector to compare the bits from the enable register to the select bits from the bit shifter to provide an error signal indicating an attempt to access a segment that is currently not enabled.

14. The apparatus of claim 1, wherein the comparison logic is adapted to compensate for the allocation of memory for the segments of the block of memory by an operating system in response to a request by an application.

15. The apparatus of claim 1, wherein the apparatus is a channel adapter.

16. A system comprising:

an operating system;

a system memory; and

a channel adapter operatively coupled to the operating system, wherein the channel adapter includes comparison logic to determine which segment of multiple segments of a block of memory in the system memory is being addressed by a received index and to generate the physical address of the location in the block of memory for the received index, the comparison logic adapted to compensate for the block of memory having a segment that is non-contiguous with the other segments of the block of memory to access the block of memory as a single contiguous block of memory.

17. The system of claim 16, wherein the channel adapter includes a number of first registers, each first register to contain a value denoting a size of a corresponding segment of the multiple segments of the block of memory.

18. The system of claim 17, wherein the channel adapter includes a number of second registers, each of the second registers to contain a value denoting a starting physical address of an associated segment of the multiple segments of the block of memory.

19. The system of claim 18, wherein the comparison logic is adapted to generate the physical address of the location in the block of memory for the received index by using

the size of each segment logically preceding the segment determined to be addressed by the received index.

20. The system of claim 18, wherein the comparison logic is adapted to generate the physical address of the location in the block of memory for the received index by adding the received index to the starting physical address of the segment determined to be addressed by the received index after subtracting the sizes of the segments logically preceding the segment determined to be addressed by the received index.

21. The system of claim 18, wherein the comparison logic further includes an enable register, the enable register containing a bit for each of the multiple segments of the block of memory, each bit denoting whether the associated segment of the multiple segments of the block of memory is enabled, the enable register being software programmable.

22. The system of claim 16, wherein the channel adapter is a target channel adapter.

23. A method comprising:

determining which segment of multiple segments of a block of memory is being addressed by a received index; and

generating a physical address of the location in the block of memory for the received index, wherein generating the physical address compensates for the block of memory having a segment that is non-contiguous with the other segments of the block of memory to access the block of memory as a single contiguous block of memory.

24. The method of claim 23, wherein the method further includes dynamically allocating memory to a segment of the block of memory.

25. The method of claim 23, wherein the method further includes:

storing a size for each of the segments of the block of memory; and

storing a base address for each segment, each base address denoting the starting

physical address of the associated segment of the block of memory.

26. The method of claim 25, wherein generating a physical address of the location in the block of memory for the received index includes generating the physical address by adding the received index to a base address.

27. The method of claim 25, wherein generating a physical address of the location in the block of memory for the received index includes using the size of each segment logically preceding the segment determined to be addressed by the received index.

28. The method of claim 25, wherein generating a physical address of the location in the block of memory for the received index includes adding the received index to the base address of the segment determined to be addressed by the received index after subtracting the sizes of the segments logically preceding the segment determined to be addressed by the received index.

29. The method of claim 25, wherein the method further includes disabling a segment of the multiple segments of the block of memory.

30. The method of claim 25, wherein the method further includes detecting an attempt to access a segment that is disabled and providing error signal indicating the attempted access to the disabled segment.

31. A computer-readable medium having computer-executable instructions for performing a method comprising:

determining which segment of multiple segments of a block of memory is being addressed by a received index; and

generating a physical address of the location in the block of memory for the received index, wherein generating the physical address compensates for the block of memory having a segment that is non-contiguous with the other segments of the block of memory to access the block of memory as a single contiguous block of memory.

32. The computer-readable medium of claim 31, wherein the computer-readable medium has computer-executable instructions for performing the method further including dynamically allocating memory to a segment of the block of memory.

33. The computer-readable medium of claim 31, wherein the computer-readable medium has computer-executable instructions for performing the method further including:

storing a size for each of the segments of the block of memory; and

storing a base address for each segment, each base address denoting the starting physical address of the associated segment of the block of memory.

34. The computer-readable medium of claim 33, wherein generating a physical address of the location in the block of memory for the received index includes generating the physical address by adding the received index to a base address.

35. The computer-readable medium of claim 33, wherein generating a physical address of the location in the block of memory for the received index includes using the size of each segment logically preceding the segment determined to be addressed by the received index.

36. The computer-readable medium of claim 33, wherein generating a physical address of the location in the block of memory for the received index includes adding the received index to the base address of the segment determined to be addressed by the received index after subtracting the sizes of the segments logically preceding the segment determined to be addressed by the received index.

37. The computer-readable medium of claim 33, wherein the computer-readable medium has computer-executable instructions for performing the method further including disabling a segment of the multiple segments of the block of memory.

38. The computer-readable medium of claim 33, wherein the computer-readable medium has computer-executable instructions for performing the method further including detecting an attempt to access a segment of the multiple segments of the block of memory that is disabled and providing error signal indicating the attempted access to the disabled segment.